REMARKS

Claims 1 to 12 were pending when last examined. Applicant has amended claim 1 and canceled claims 3 and 7 to 12.

Drawings

The Examiner objected to the drawings because they fail to illustrate a single parity bit that could be used for the combined tag and data parity as recited in claim 9. Applicant has canceled claim 9, thereby rendering this objection moot. Nonetheless, Applicant notes that the Specification states that "[t]his combined parity bit(s) could be stored in either the data store 55 or the tag memory 60," which is illustrated in Fig. 2 as both data store 55 and tag memory 60 are shown to have an area for storing parity data. Specification, paragraph 19.

§102 Rejections

U.S. Patent No. 5,479,641 ("Nadir et al.")

The Examiner rejected claims 1, 3 to 8, and 12 under 35 U.S.C. § 102(b) as being anticipated by Nadir et al.

Applicant has amended claim 1 to include the limitations of claim 3, and canceled claim 3. Amended claim 1 now recites:

> 1. A method for error protection of a cache memory, wherein each entry in a tag memory and a data store within the cache memory associates with a parity bit, comprising:
>
> (a) providing a read request to a system memory associated with the cache memory, the read request correlating to an entry in the tag memory and the data store;
>
> (b) checking the parity bit associated with the correlated entry in the tag memory and the parity bit associated with the correlated entry in the data store;
>
> (c) if either act (a) or act (b) indicates an error in the corresponding correlated entry, declaring a miss; and
>
> (d) invalidating the correlated entry in the data store if a miss is declared in act (c).

Amended claim 1 (emphasis added).

Regarding original claim 3, now incorporated into amended claim 1, the Examiner stated, "Nadir teaches invalidating the correlated entry in the data store if a miss is declared in act(c) in

col. 9 lines 18-20 and lines 46-49." July 15, 2004 Office Action, p. 4. Applicant respectfully traverses.

Nadir et al. does not teach that the cache line is declared invalid when there is a data parity error because the detailed description of Nadir et al. does not disclose a data parity bit. Instead, the detailed description of Nadir et al. discloses a validity bit that is derived from the tag parity bit.

> Preceding from the decision 230, if there is a parity error then operation moves to a box 238 in which the read operation is aborted and the selected cache line is marked invalid. Subsequently, operation moves to a box 239 in which a memory cycle is performed to get data.

Nadir et al., col. 9, lines 31 to 50. Tracing backwards from boxes 238 and 230 on Fig. 4B to Fig. 4A, it can be seen that the parity error referred to in the above-quote paragraph comes from box 218 where a stored parity bit from box 214 and a newly generated parity bit from box 216 are compared. In box 214, a stored parity bit 76 for a tag address is retrieved from a status array 64. In box 216, a parity bit is generated from the tag address.

> The enabled tag field is also supplied to the box 216 in which parity is generated to supply a generated tag parity signal which in turn is supplied to a box 218 in which the generated parity is compared with the enabled parity field.

Nadir et al., col. 9, lines 25 to 29. Thus, Nadir et al. only discloses invalidating a cache line for tag parity errors and not either tag parity errors or data parity errors.

Claims 4 to 6 depend from claim 1 and are patentable over Nadir et al. for at least the same reasons as amended claim 1.

Applicant has canceled claims 7, 8, and 12, thereby rendering their rejections moot.

U.S. Patent No. 5,345,582 ("Tsuchiya")

The Examiner rejected claims 7 and 9 under 35 U.S.C. § 102(b) as being anticipated by Tsuchiya. Applicant has canceled claims 7 and 9, thereby rendering their rejections moot.

§ 103 Rejections

The Examiner rejected claims 2, 10, and 11 under § 103(a) as being unpatentable over Nadir et al. in view of the other cited references.

Claim 2 depends from amended claim 1 and is patentable over the combination of the cited references for at least the same reasons as claim 1.

Applicant has canceled claims 10 and 11, thereby rendering their rejections moot.

In summary, claims 1 to 12 were pending when last examined. Applicant has amended claim 1 and canceled claims 3 and 7 to 12. For the above reasons, Applicant respectfully requests allowance of claims 1, 2, 4 to 6. Should the Examiner have any questions, please call the undersigned at (408) 382-0480 x206.

Certification of Facsimile Transmission

I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature 10/15/2004 Date

Respectfully submitted,

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